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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,203	01/30/2004	Lee-Yeun Hwang	0630-1951P	5731

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,203	HWANG, LEE-YEUN	
	Examiner.	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/863,452.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 9-12, and 16-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert (U.S. 5,869,875) in view of Malhi (U.S. 5,640,034).

Regarding claim 1, Hebert teaches a high-voltage device, comprising an n-type drift region (**18** in Fig. 3) and a p-type drift region (**24** in Fig. 3) on a substrate (**12** in Fig. 3); a gate region defined at an intersection between the n and p-type drift region, the gate region having an oxide film (labeled "oxide" in Fig. 3) on an upper portion of the gate region and a gate electrode formed on the oxide film (labeled "Gate" in Fig. 3); a source region being defined in one of the n and p-type drift regions, the source region having a first trench filled with a first polysilicon layer (**30** in Fig. 3), a first high-density diffusion layer formed on an upper portion of the first polysilicon layer (**14** in Fig. 3—absent disclosure of the unexpected results or critical nature of forming the n-type diffusion layer on the polysilicon layer, the formation of the n-type diffusion layer directly adjacent to, and in electrical contact with, the polysilicon layer is deemed equivalent. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990)), and a source electrode formed on the high-density diffusion layer (**50** in Fig. 5E); and a drain region being defined in the other of the n and p-type drift regions, the drain region

having a second high-density diffusion layer formed on an upper part of the drain region (**16** in Fig. 3) and a drain electrode formed on the second high-density diffusion layer (**52** in Fig. 5E).

Hebert does not teach a second polysilicon layer filling a second trench formed between the n and p-type drift regions of the gate region such that the oxide film is deposited in the second trench as well as the upper portion of the drift region corresponding to the drain region.

Malhi teaches forming a trench in a gate region of a LDMOS that is subsequently filled with polysilicon (Fig. 2; column 2, lines 27-34). The gate oxide film is deposited in this trench as well as the upper portion of the drain region (see Fig. 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the device taught by Hebert by incorporating a trench in the gate region, as taught by Malhi. The motivation for doing so at the time of the invention would have been to reduce the device's "on-resistance," as expressly taught by Malhi (column 1, lines 32-34).

Regarding claim 3, Hebert and Malhi together teach the high-voltage device according to claim 1. Hebert further teaches that the first polysilicon is formed in the first trench such that a depth of the first trench is substantially equal to a depth of the one of the n and p-type drift region where the source region is defined (Fig. 3).

Regarding claim 4, Hebert and Malhi together teach the high-voltage device according to claim 1. Hebert further teaches that the first trench is formed at the p-type drift region (Fig. 3).

Regarding claims 5 and 6, Hebert and Malhi together teach the high-voltage device according to claim 4. Hebert further teaches that the first and second high-density diffusion layers are n+ layers (column 2, lines 11-13).

Regarding claims 9 and 16, Hebert teaches a high-voltage device and a method for forming the high-voltage device, the device comprising a substrate (**12** in Fig. 3); a first drift region (**24** in Fig. 3) and a second drift region (**18** in Fig. 3) formed in the substrate; a gate electrode (labeled "Gate" in Fig. 3) formed over a gate region, the gate region being defined over an intersection of said first and second drift regions such that the gate region includes a part of said first drift region and a part of said second drift region (Fig. 3); a first polysilicon layer (**30** in Fig. 3) filling a first trench formed in a source region, the source region being defined in said first drift region; a first high-density diffusion layer (**14** in Fig. 3) formed in an upper portion of the source region including a portion of the first polysilicon layer and a portion of the first drift region in between the first trench and the gate region (absent disclosure of the unexpected results or critical nature of forming the n-type diffusion layer on the polysilicon layer, the formation of the n-type diffusion layer directly adjacent to, and in electrical contact with, the polysilicon layer is deemed equivalent. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990)); and a second high-density diffusion layer formed in a drain region, the drain region being defined in the second drift region (**16** in Fig. 3).

Hebert does not teach an oxide film formed in a second trench formed in the gate region, the oxide film also formed on an upper portion of the gate region in between the second trench and the drain region; and a second polysilicon layer filling the second

trench covering the oxide film formed within the second trench such that the gate electrode covers at least a portion of the second polysilicon layer and the oxide film on the upper portion of the gate region.

Malhi teaches forming a trench in a gate region of a LDMOS that is subsequently filled with polysilicon (Fig. 2; column 2, lines 27-34). The gate oxide film is deposited in this trench as well as the upper portion of the drain region, in between the trench and the drain region (see Fig. 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the device taught by Hebert by incorporating a trench in the gate region, as taught by Malhi. The motivation for doing so at the time of the invention would have been to reduce the device's "on-resistance," as expressly taught by Malhi (column 1, lines 32-34).

Regarding claims 10 and 17, Hebert and Malhi together teach the high-voltage device of claim 9 and the method of claim 16. Hebert further teaches that the first drift region is p-type and the second drift region is n-type (Fig. 3).

Regarding claims 11, 12, 18, and 19, Hebert and Malhi together teach the high-voltage device of claim 9 and the method of claim 16. Hebert further teaches that the first and second high-density diffusion layers are n-type (column 2, lines 11-13).

Claims 7, 8, 13, 14, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert (U.S. 5,869,875) in view of Malhi (U.S. 5,640,034), as applied to claims 5, 9, and 16, and further in view of applicant's admitted prior art (APA).

Regarding claims 7, 8, 13, 14, 20, and 21, Hebert and Malhi together teach the high-voltage device according to claims 5 and 9 and the method of claim 16, but do not teach a third high-density diffusion layer in the source region adjacent to the first high-density layer, or that the third high-density diffusion layer is a p+ layer.

However, APA teaches a p+ high-density diffusion layer (**8** in Fig. 1A, **8'** in Fig. 2, paragraph 0009-0013 of the instant specification) in the source region adjacent the first high-density layer. This layer mitigates the lowering of the maximum operating voltage caused by a latch-up phenomenon (paragraph 0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the device taught by Hebert and Malhi together by adding a third high-density diffusion layer in the source region adjacent the first high-density layer, wherein the third high-density diffusion layer is a p+ layer, as taught by APA. The motivation for doing so at the time of the invention would have been to mitigate the lowering of the maximum operating voltage cause by a latch-up phenomenon, as expressly taught by APA.

Response to Arguments

Applicant's arguments filed 1/13/2006 have been fully considered but they are not persuasive.

Regarding the combination of Hebert and Malhi to reject claims 1, 9, and 16, Applicant argues that Hebert does not disclose that the second polysilicon layer is filled within the second trench formed between the N and P-type drift regions of the gate, and that Malhi does not disclose that the source region has a first trench filled with the first

polysilicon layer and the source electrode formed on the high density diffusion layer (see first full paragraph on page 10).

However, Hebert does teach that the gate area is in a region defined at an intersection between an N- and P-type drift region, and Malhi teaches forming a trench in a gate region such that the gate oxide film is deposited in the trench, and filling the trench with polysilicon. Hebert already teaches that the oxide film is deposited on the upper portion of the drift region corresponding to the drain region. Additionally, although Malhi does not disclose a first trench filled with polysilicon in the source region, and the source electrode formed on the high-density diffusion layer, Hebert does (see rejection of claim 1 above). Since the rejection is based upon the combined teachings of Hebert and Malhi, it is not necessary for each reference to teach every feature of the claim.

Regarding claims 7, 8, 13, 14, 20, and 21, Applicant argues that it is not proper to use Applicant's disclosure of conventional art as admitted prior art, since Applicant only admits that it is conventional, and not necessarily statutory prior art (see the last paragraph on page 10 and page 11).

However, this argument is not persuasive because an admission in the disclosure that features of an invention are conventional is an admission that the features are not novel, and therefore not patentable, which is an appropriate argument to use in a rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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